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EXAMINER	
DAY, HERNG DER	

ART UNIT	PAPER NUMBER
2128	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/087,069	JAKATDAR ET AL.	
	Examiner	Art Unit	
	Herng-der Day	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 February 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-52* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-52* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/2/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-52 have been examined and claims 1-52 have been rejected.

Abstract

2. The abstract of the disclosure is objected to because it exceeds 150 words in length. Correction is required. See MPEP § 608.01(b).

Specification

3. The disclosure is objected to because of the following informalities. Appropriate correction is required.

3-1. Please update the status regarding co-pending U.S. patent applications in the specification.

3-2. It appears that "Figures 4 to 8C", as described in line 3 of paragraph [0028], should be "Figures 4 to 8B" because Figure 8C does not exist.

3-3. It appears that "Simulation type is this case", as described in line 21 of paragraph [0035], should be "Simulation type in this case".

3-4. It appears that "generating a response 209", as described in line 5 of paragraph [0043], should be "generating a response 213".

Claim Rejections - 35 USC § 101

4. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

5. Claims 51-52 are rejected under 35 U.S.C. 101 because the inventions as disclosed in claims are directed to non-statutory subject matter.

5-1. Regarding claims 51-52, it appears to be directed merely to a simulation data store comprising one or more instances of a simulation data store. Therefore, the precise structure of the instances of a simulation data store is software programming per se. In other words, the claimed invention taken as a whole is directed to a mere program/data listing and hence nonstatutory.

5-2. The Examiner acknowledges that even though the claims are presently considered non-statutory they are additionally rejected below over the prior art. The Examiner assumes the Applicants will amend the claims to overcome the 101 rejections and thus make the claims statutory.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-9, 11, 13, 16, 18, 19, and 21-52 are rejected under 35 U.S.C. 102(b) as being anticipated by Chen, U.S. Patent 5,719,796 issued February 17, 1998.

7-1. Regarding claim 1, Chen discloses a method of creating a profile-based simulation data store for an integrated circuit utilizing one or more simulations, the method comprising:

simulating one or more fabrication processes using a selected set of process control parameters (A simulation start step 452 begins the simulation process 450 in response to initializing data from the actual in-line process 420, column 6, lines 36-54), the fabrication process simulations generating fabrication attributes (Simulation results from the simulation step 454, column 7, lines 31-36);

generating calculated signals with a metrology simulator (A conversion operation is performed on the simulated profile in matching process conversion step 468, column 8, lines 4-25), the metrology simulator using profile data from the fabrication attributes (The generate simulated profile step 458 constructs a simulated profile, column 7, lines 36-41), the profile data comprising profile shapes and critical dimensions of structures resulting from the one or more fabrication process simulations (vertical dimension data and horizontal dimension data, column 6, lines 19-25); and

creating simulation data store instances, the instances including profile data and corresponding calculated signals, simulation types, and associated process control parameters and fabrication attributes (Output data that is generated by the calibration process 400 includes all of the matching profiles and all simulated profiles, column 9, lines 1-3; profiles and data which are entered into the database, column 12, lines 14-21);

wherein the simulation types are characterizations of the one or more simulations performed (a plurality of suitable process steps is performed independently, column 6, lines 8-19).

7-2. Regarding claim 2, Chen further discloses wherein simulating one or more fabrication processes comprises:

simulating a thin film, deposition or chemical mechanical polishing process (deposition equipment, column 5, lines 2-6) using a selected first set of process control parameters (each with corresponding actual measurements (both process parameters and in-line/WET data) 314, column 5, lines 47-50); and

simulating lithography process (photolithography equipment, column 5, lines 2-6) using a selected second set of process control parameters (each with corresponding actual measurements (both process parameters and in-line/WET data) 314, column 5, lines 47-50).

7-3. Regarding claim 3, Chen further discloses wherein simulating one or more fabrication processes comprises:

simulating a lithography process (photolithography equipment, column 5, lines 2-6) using a selected first set of process control parameters (each with corresponding actual measurements (both process parameters and in-line/WET data) 314, column 5, lines 47-50); and

simulating an etch process (wet etching equipment, column 5, lines 2-6) using a selected second set of process control parameters (each with corresponding actual measurements (both process parameters and in-line/WET data) 314, column 5, lines 47-50).

7-4. Regarding claim 4, Chen further discloses wherein simulating one or more fabrication processes comprises:

simulating a lithography process (photolithography equipment, column 5, lines 2-6) using a selected first set of process control parameters (each with corresponding actual measurements (both process parameters and in-line/WET data) 314, column 5, lines 47-50); and

simulating an implantation process (ion implantation equipment, column 5, lines 2-6) using a selected second set of process control

parameters (each with corresponding actual measurements (both process parameters and in-line/WET data) 314, column 5, lines 47-50).

7-5. Regarding claim 5, Chen further discloses wherein simulating one or more fabrication processes comprises:

simulating an etch process (wet etching equipment, column 5, lines 2-6) using a selected first set of process control parameters (each with corresponding actual measurements (both process parameters and in-line/WET data) 314, column 5, lines 47-50); and

simulating a photoresist stripping process (wafer cleaning equipment, column 5, lines 2-6) using a selected second set of process control parameters (each with corresponding actual measurements (both process parameters and in-line/WET data) 314, column 5, lines 47-50).

7-6. Regarding claim 6, Chen further discloses wherein simulating one or more fabrication processes comprises:

simulating an implantation process (ion implantation equipment, column 5, lines 2-6) using a selected first set of process control parameters (each with corresponding actual measurements (both process parameters and in-line/WET data) 314, column 5, lines 47-50); and

simulating a photoresist stripping process (wafer cleaning equipment, column 5, lines 2-6) using a selected second set of process control parameters (each with corresponding actual measurements (both process parameters and in-line/WET data) 314, column 5, lines 47-50).

7-7. Regarding claim 7, Chen discloses a method of creating a profile-based simulation data store for an integrated circuit utilizing one or more simulations, the method comprising:

simulating one or more devices using a selected set of input parameters, the device simulations generating device attributes, the set of input parameters including profile data

corresponding to the one or more simulated devices (a full device simulation step 471 is performed, column 8, lines 46-54);

generating calculated signals with a metrology simulator, the metrology simulator using profile data corresponding to the one or more simulated devices (A conversion operation is performed on the simulated WET data in WET statistical profile conversion step 480, column 8, lines 54-67); and

creating simulation data store instances, the instances including profile data and corresponding calculated signals, simulation types, process control parameters, and fabrication attributes (Output data that is generated by the calibration process 400 includes all of the matching profiles and all simulated profiles, column 9, lines 1-3; profiles and data which are entered into the database, column 12, lines 14-21);

wherein the simulation types are characterizations of the one or more simulations performed (a full device simulation step 471 is performed, column 8, lines 46-54).

7-8. Regarding claim 8, Chen further discloses wherein the selected set of input parameters comprises a profile library having profile data, the profile data including profiles of the one or more devices simulated (database 1020, column 12, lines 14-21).

7-9. Regarding claim 9, Chen discloses a method of creating a profile-based simulation data store for an integrated circuit utilizing one or more simulations, the method comprising:

simulating one circuit using a selected set of input parameters, a circuit having one device, the circuit simulations generating circuit attributes, the set of input parameters including profile data corresponding to the one or more devices of the simulated one or more circuits (a full device simulation step 471 is performed, column 8, lines 46-54);

generating calculated signals with a metrology simulator, the metrology simulator using profile data corresponding to the one or more devices of the simulated one or more circuits (A conversion operation is performed on the simulated WET data in WET statistical profile conversion step 480, column 8, lines 54-67); and

creating simulation data store instances, the instances including calculated signals, profile data, simulation types, process control parameters, and circuit attributes (Output data that is generated by the calibration process 400 includes all of the matching profiles and all simulated profiles, column 9, lines 1-3; profiles and data which are entered into the database, column 12, lines 14-21);

wherein the simulation types are characterizations of the one or more simulations performed (a full device simulation step 471 is performed, column 8, lines 46-54).

7-10. Regarding claim 11, Chen discloses a method of creating a profile-based simulation data store for an integrated circuit utilizing one or more simulations, the method comprising:

simulating one or more fabrication processes using a selected set of process control parameters (A simulation start step 452 begins the simulation process 450 in response to initializing data from the actual in-line process 420, column 6, lines 36-54), the fabrication process simulations generating fabrication attributes (Simulation results from the simulation step 454, column 7, lines 31-36);

generating calculated signals with a metrology simulator (A conversion operation is performed on the simulated profile in matching process conversion step 468, column 8, lines 4-25), the metrology simulator using profile data from the generated fabrication attributes (The generate simulated profile step 458 constructs a simulated profile, column 7, lines 36-41), the

profile data comprising profile shapes and critical dimensions of structures resulting from the one or more fabrication process simulations (vertical dimension data and horizontal dimension data, column 6, lines 19-25); and

simulating one or more devices using profile data generated by the one or more simulated fabrication processes (a full device simulation step 471 is performed, column 8, lines 46-54); and

creating simulation data store instances, the instances including profile data from the generated fabrication attributes, corresponding calculated signals, simulation types and associated process control parameters and device attributes (Output data that is generated by the calibration process 400 includes all of the matching profiles and all simulated profiles, column 9, lines 1-3; profiles and data which are entered into the database, column 12, lines 14-21);

wherein the simulation types are characterizations of the one or more simulations performed (a plurality of suitable process steps is performed independently, column 6, lines 8-19; a full device simulation step 471 is performed, column 8, lines 46-54).

7-11. Regarding claim 13, Chen discloses a method of creating a profile-based simulation data store for an integrated circuit, the method comprising:

simulating one or more devices using a selected set of input parameters, the device simulations generating device attributes, the set of input parameters including profile data of the one or more simulated devices (a full device simulation step 471 is performed, column 8, lines 46-54);

generating calculated signals with a metrology simulator, the metrology simulator using profile data of the one or more simulated devices (A conversion operation is performed on the simulated WET data in WET statistical profile conversion step 480, column 8, lines 54-67);

simulating one or more circuits using the generated device attributes from the one or more device simulations as input parameters, the circuit simulations generating circuit attributes (a full device simulation step 471 is performed, column 8, lines 46-54); and

creating simulation data store instances, the instances including profile data and corresponding calculated signals, simulation types and associated input parameters, device attributes, and circuit attributes (Output data that is generated by the calibration process 400 includes all of the matching profiles and all simulated profiles, column 9, lines 1-3; profiles and data which are entered into the database, column 12, lines 14-21);

wherein the simulation types are characterizations of the one or more simulations performed (a plurality of suitable process steps is performed independently, column 6, lines 8-19; a full device simulation step 471 is performed, column 8, lines 46-54).

7-12. Regarding claim 16, Chen discloses a method of creating a profile-based simulation data store for an integrated circuit utilizing one or more simulations, the method comprising:

simulating one or more fabrication processes using a selected set of process control parameters (A simulation start step 452 begins the simulation process 450 in response to initializing data from the actual in-line process 420, column 6, lines 36-54), the fabrication process simulations generating fabrication attributes (Simulation results from the simulation step 454, column 7, lines 31-36);

generating calculated signals with a metrology simulator (A conversion operation is performed on the simulated profile in matching process conversion step 468, column 8, lines 4-25), the metrology simulator using profile data from the fabrication attributes (The generate simulated profile step 458 constructs a simulated profile, column 7, lines 36-41), the profile data

comprising profile shapes and critical dimensions of structures resulting from the one or more fabrication process simulations (vertical dimension data and horizontal dimension data, column 6, lines 19-25);

simulating one or more devices using profile data generated by the one or more simulated fabrication processes (a full device simulation step 471 is performed, column 8, lines 46-54);

simulating one circuit using the generated device attributes from the one or more device simulations as input parameters, the circuit simulations generating circuit attributes (a full device simulation step 471 is performed, column 8, lines 46-54); and

creating simulation data store instances, the instances including profile data, corresponding calculated signals, simulation types, and associated process control parameters, fabrication attributes, device attributes, and circuit attributes (Output data that is generated by the calibration process 400 includes all of the matching profiles and all simulated profiles, column 9, lines 1-3; profiles and data which are entered into the database, column 12, lines 14-21);

wherein the simulation types are characterizations of the one or more simulations performed (a plurality of suitable process steps is performed independently, column 6, lines 8-19; a full device simulation step 471 is performed, column 8, lines 46-54).

7-13. Regarding claim 18, Chen discloses a method of creating a profile-based simulation data store for an integrated circuit, the method comprising:

measuring one or more test gratings with a metrology device wherein the test gratings model the effect of an integrated circuit design and/or fabrication process (the in-line measurement step 426 measures the data profile, column 7, lines 61-64);

generating measured signals with the metrology device (The actual data to simulated data comparison step 462 receives ... actual in-line data from the in-line measurement step 426, column 7, line 64, through column 8, line 1);

converting the measured signals into profile data corresponding to the measured test gratings (conversion step 468, column 8, lines 4-25);

simulating one or more devices using the converted profile data as a set of input parameters, the device simulations generating device attributes (a full device simulation step 471 is performed, column 8, lines 46-54); and

creating simulation data store instances, the instances including profile data, corresponding measured signals, simulation types, and associated device attributes (Output data that is generated by the calibration process 400 includes all of the matching profiles and all simulated profiles, column 9, lines 1-3; profiles and data which are entered into the database, column 12, lines 14-21);

wherein the simulation types are characterizations of the one or more simulations performed (a plurality of suitable process steps is performed independently, column 6, lines 8-19).

7-14. Regarding claim 19, Chen further discloses wherein converting the measured signals into process control parameters further comprises:

comparing the measured signals off the test gratings to instances of a library of calculated signals, the instances of the library of calculated signals having data elements comprising calculated signals and profile data (an actual data to simulated data comparison step 462, column 7, lines 61-64);

selecting corresponding best matching instances in the library of calculated signals; and accessing profile data from the selected best matching instances of the library of calculated signals (determine best fit step 822, column 10, lines 59-62).

7-15. Regarding claim 21, Chen further discloses wherein measuring the test grating further comprises:

designing the test gratings to capture interconnect geometric configurations of the integrated circuit (vertical dimension data and horizontal dimension data, column 6, lines 19-25);

fabricating the desired test gratings (a single process step 424 for performing a single selected fabrication process step, column 6, lines 1-4); and

measuring the fabricated test gratings with the metrology device (a measurement step 426 for measuring a result of the selected fabrication process, column 6, lines 1-5).

7-16. Regarding claim 22, Chen further discloses wherein the device attributes include resistance, inductance, capacitance, potential, temperature, and current density distribution of the interconnect (A generate device simulation profile step 473 generates a device profile that corresponds to the actual calculated WET data, column 8, lines 46-54).

7-17. Regarding claim 23, Chen discloses a method of real-time use of simulation data store, the method comprising:

measuring a grating with a metrology device, the grating modeling an interconnect geometry of an integrated circuit, the measurement generating a measured signal (generates ... information for derivation of WET data measurement step 1016, column 7, lines 61-64); and

obtaining interconnect electrical properties and/or thermal properties corresponding to the measured signal off the grating (This WET data is assembled in WET data block 1018, column 12, lines 13-15).

7-18. Regarding claim 24, Chen further discloses wherein obtaining interconnect electrical properties and/or thermal properties corresponding to the measured signal off the grating further comprises:

accessing a simulation data store, the simulated data store storing instances having data elements comprising signals and device attributes, the device attributes including interconnect electrical properties and/or thermal properties (database 1020, column 12, lines 14-21);

comparing the measured signal to the signals in the instances of the simulation data store (a calibration process 1026, column 12, lines 14-19);

selecting a best matching instance of the simulation data store; and accessing the interconnect electrical properties and/or thermal properties associated with the best matching instance of the simulated data store (determine best fit step 822, column 10, lines 59-62).

7-19. Regarding claim 25, Chen further discloses wherein the interconnect electrical properties include capacitance, inductance, and resistance (A generate device simulation profile step 473 generates a device profile that corresponds to the actual calculated WET data, column 8, lines 52-54).

7-20. Regarding claim 26, Chen discloses a method of creating a profile-based simulation data store for an integrated circuit utilizing a metrology simulator, the method comprising:

performing fabrication process simulations using a set of process control parameters (A simulation start step 452 begins the simulation process 450 in response to initializing data from

the actual in-line process 420, column 6, lines 36-54), the fabrication process simulations generating a set of fabrication attributes and a set of structure profile data (The generate simulated profile step 458 constructs a simulated profile, column 7, lines 36-41);

calculating a set of simulated signals corresponding to the set of structure profile data using a metrology simulator (A conversion operation is performed on the simulated profile in matching process conversion step 468, column 8, lines 4-25); and

creating instances of a simulation data store, each instance of the simulation data store having data elements comprising profile data and corresponding calculated signals, simulation types, and associated process control parameters and fabrication attributes (Output data that is generated by the calibration process 400 includes all of the matching profiles and all simulated profiles, column 9, lines 1-3; profiles and data which are entered into the database, column 12, lines 14-21);

wherein the simulation types are characterizations of the simulations performed (a plurality of suitable process steps is performed independently, column 6, lines 8-19).

7-21. Regarding claim 27, Chen further discloses wherein the fabrication process simulation is a lithography simulation (photolithography equipment, column 5, lines 2-6).

7-22. Regarding claim 28, Chen further discloses wherein the fabrication process simulation is a combined lithography and etch simulation (photolithography and wet etching equipment, column 5, lines 2-6).

7-23. Regarding claim 29, Chen further discloses wherein the fabrication process simulation is an implantation simulation, diffusion simulation, oxidation simulation, deposition and etching simulation, chemical mechanical polishing simulation, deposition and reflow simulation, 2-

dimensional process simulation, or 3-dimensional fabrication process simulation (fabrication equipment 210, column 5, lines 2-6).

7-24. Regarding claim 30, Chen further discloses wherein the metrology simulator is an optical metrology simulator (test equipment 212, column 5, lines 6-11).

7-25. Regarding claim 31, Chen discloses a system for creating a profile-based simulation data store for an integrated circuit, the system comprising:

a profile application server configured to:

compare a measured signal off a test grating in a wafer to calculated signals in instances of a calculated signals library (These data are assembled in data process block 1024 and applied to a calibration process 1026, column 12, lines 14-19), the library instances storing data elements comprising calculated signals and profile data (database 1020, column 12, lines 14-21), and

select a best matching instance of the library of calculated signals (determine best fit step 822, column 10, lines 59-62);

a fabrication process simulator configured to:

simulate one or more fabrication processes (A simulation start step 452 begins the simulation process 450 in response to initializing data from the actual in-line process 420, column 6, lines 36-54), and

generate fabrication attributes utilizing profile data associated with the best matching instance of the library of calculated signals (The generate simulated profile step 458 constructs a simulated profile, column 7, lines 36-41); and

a simulation data store generator configured to;

create an instance of a simulation data store, the simulation data store instance storing data elements comprising the profile data, associated measured signals, simulation types, and the associated fabrication attributes (Output data that is generated by the calibration process 400 includes all of the matching profiles and all simulated profiles, column 9, lines 1-3; profiles and data which are entered into the database, column 12, lines 14-21);

wherein the simulation types are characterizations of the one or more fabrication processes simulations performed (a plurality of suitable process steps is performed independently, column 6, lines 8-19).

7-26. Regarding claim 32, Chen discloses a system for creating a profile-based simulation data store for an integrated circuit, the system comprising:

a profiler application server configured to;

compare a measured signal off a test grating in a wafer to calculated signals in instances of a calculated signals library (These data are assembled in data process block 1024 and applied to a calibration process 1026, column 12, lines 14-19), the library instances storing data elements comprising profile data and associated calculated signals (database 1020, column 12, lines 14-21), and

select a best matching instance of the library of calculated signals (determine best fit step 822, column 10, lines 59-62);

a device simulator configured to:

simulate one or more devices (a full device simulation step 471 is performed, column 8, lines 46-54), and

generate device attributes utilizing profile data associated with the best matching instance of the library of calculated signals (A generate device simulation profile step 473 generates a device profile that corresponds to the actual calculated WET data, column 8, lines 46-54); and

a simulation data store generator configured to:

create an instance of a simulation data store, the simulation data store instance storing data elements comprising the profile data, associated measured signals, simulation types, and associated device attributes (Output data that is generated by the calibration process 400 includes all of the matching profiles and all simulated profiles, column 9, lines 1-3; profiles and data which are entered into the database, column 12, lines 14-21);

wherein the simulation types are characterizations of the one or more device simulations performed (a full device simulation step 471 is performed, column 8, lines 46-54).

7-27. Regarding claim 33, Chen discloses a system for creating a profile-based simulation data store for an integrated circuit, the system comprising:

a profile application server configured to:

compare a measured signal off a test grating in a wafer to calculated signals in instances of a calculated signals library (These data are assembled in data process block 1024 and applied to a calibration process 1026, column 12, lines 14-19), the library instances storing data elements comprising profile data and associated calculated signals (database 1020, column 12, lines 14-21), and

select a best matching instance of the library of calculated signals (determine best fit step 822, column 10, lines 59-62);

a device simulator configured to:

simulate one or more circuits (a full device simulation step 471 is performed, column 8, lines 46-54), and

generate circuit attributes utilizing profile data associated with the best matching instance of the library of calculated signals (A generate device simulation profile step 473 generates a device profile that corresponds to the actual calculated WET data, column 8, lines 46-54); and

a simulation data store generator configured to:

create an instance of a simulation data store, the simulation data store instance storing data elements comprising the profile data, associated measured signals, simulation types, and associated circuit attributes (Output data that is generated by the calibration process 400 includes all of the matching profiles and all simulated profiles, column 9, lines 1-3; profiles and data which are entered into the database, column 12, lines 14-21);

wherein the simulation types are characterizations of the one or more circuit simulations performed (a full device simulation step 471 is performed, column 8, lines 46-54).

7-28. Regarding claim 34, Chen discloses a system for creating a profile-based simulation data store for an integrated circuit, the system comprising:

a fabrication process simulator configured to:

simulate one or more fabrication processes using a selected set of process control parameters (A simulation start step 452 begins the simulation process 450 in response to initializing data from the actual in-line process 420, column 6, lines 36-54), the fabrication process simulations generating fabrication attributes (Simulation results from the simulation step

454, column 7, lines 31-36), the fabrication attributes including structure profile data (The generate simulated profile step 458 constructs a simulated profile, column 7, lines 36-41);

a metrology simulator configured to:

receive the structure profile data from the fabrication process simulator (The actual data to simulated data comparison step 462 receives simulated data from the generate simulated profile step 458, column 7, line 64, through column 8, line 1), and

generate calculated metrology signals using a simulated grating, the simulated grating having a repeating structure with the same profile data as the received structure profile data (A conversion operation is performed on the simulated profile in matching process conversion step 468, column 8, lines 4-25);

a simulation data store generator configured to:

create instances of a simulation data store, each simulation data store instance storing data elements comprising the profile data, associated calculated signals, simulation types, and associated process control parameters and fabrication attributes (Output data that is generated by the calibration process 400 includes all of the matching profiles and all simulated profiles, column 9, lines 1-3; profiles and data which are entered into the database, column 12, lines 14-21);

wherein the simulation types are characterizations of the one or more fabrication process simulations performed (a plurality of suitable process steps is performed independently, column 6, lines 8-19).

7-29. Regarding claim 35, Chen discloses a system for creating a profile-based simulation data store for an integrated circuit, the system comprising:

a fabrication process simulator configured to:

simulate one or more fabrication processes using a selected set of process control parameters (A simulation start step 452 begins the simulation process 450 in response to initializing data from the actual in-line process 420, column 6, lines 36-54), the fabrication process simulations generating fabrication attributes (Simulation results from the simulation step 454, column 7, lines 31-36), the generated fabrication attributes including structure profile data (The generate simulated profile step 458 constructs a simulated profile, column 7, lines 36-41);

a metrology simulator configured to:

receive the structure profile data from the fabrication process simulator (The actual data to simulated data comparison step 462 receives simulated data from the generate simulated profile step 458, column 7, line 64, through column 8, line 1), and

generate calculated metrology signals using a simulated grating, the simulated grating having a repeating structure with the same profile data as the received structure profile data (A conversion operation is performed on the simulated profile in matching process conversion step 468, column 8, lines 4-25);

a device simulator configured to:

simulate one or more devices using the profile data from the generated fabrication attributes (a full device simulation step 471 is performed, column 8, lines 46-54);

a simulation data store generator configured to:

create instances of a simulation data store, each simulation data store instance storing data elements comprising the profile data, associated measured signals, simulation types, and associated process control parameters, fabrication attributes, and device attributes (Output

data that is generated by the calibration process 400 includes all of the matching profiles and all simulated profiles, column 9, lines 1-3; profiles and data which are entered into the database, column 12, lines 14-21);

wherein the simulation types are characterizations of the one or more fabrication or device simulations performed (a plurality of suitable process steps is performed independently, column 6, lines 8-19; a full device simulation step 471 is performed, column 8, lines 46-54).

7-30. Regarding claim 36, Chen discloses a system for creating a profile-based simulation data store for an integrated circuit, the system comprising:

a fabrication process simulator configured to:

simulate one or more fabrication processes using a selected set of process control parameters (A simulation start step 452 begins the simulation process 450 in response to initializing data from the actual in-line process 420, column 6, lines 36-54), the fabrication process simulations generating fabrication attributes (Simulation results from the simulation step 454, column 7, lines 31-36), the generated fabrication attributes including structure profile data (The generate simulated profile step 458 constructs a simulated profile, column 7, lines 36-41);

a metrology simulator configured to:

receive the structure profile data from the fabrication process simulator (The actual data to simulated data comparison step 462 receives simulated data from the generate simulated profile step 458, column 7, line 64, through column 8, line 1), and

generate calculated metrology signals using a simulated grating, the simulated grating having a repeating structure with the same profile data as the corresponding received

structure profile data (A conversion operation is performed on the simulated profile in matching process conversion step 468, column 8, lines 4-25);

a device simulator configured to:

simulate one or more devices using the profile data from the generated fabrication attributes, the one or more device simulations generating device attributes (a full device simulation step 471 is performed, column 8, lines 46-54);

a circuit simulator configured to:

simulate one or more circuits using the generated device attributes from the one or more device simulations as input parameters, the one or more circuit simulations generating circuit attributes (a full device simulation step 471 is performed, column 8, lines 46-54);

a simulation data store generator configured to:

create instances of a simulation data store, each simulation data store instance storing data elements comprising the profile data, associated measured signals, simulation types, and associated process control parameters, fabrication attributes, device attributes, and circuit attributes (Output data that is generated by the calibration process 400 includes all of the matching profiles and all simulated profiles, column 9, lines 1-3; profiles and data which are entered into the database, column 12, lines 14-21);

wherein the simulation types are characterizations of the one or more fabrication process, device or circuit simulations performed (a plurality of suitable process steps is performed independently, column 6, lines 8-19; a full device simulation step 471 is performed, column 8, lines 46-54).

7-31. Regarding claim 37, Chen discloses a system for creating a profile-based simulation data store for an integrated circuit, the system comprising:

a metrology simulator configured to:

generate calculated metrology signals using input profile data (A generate device simulation profile step 473 generates a device profile that corresponds to the actual calculated WET data, column 8, lines 46-54);

a device simulator configured to:

simulate one or more devices using the input profile data, the one or more device simulations generating device attributes (a full device simulation step 471 is performed, column 8, lines 46-54);

a circuit simulator configured to:

simulate one or more circuits using the generated device attributes from the one or more device simulations as input parameters, the one or more circuit simulations generating circuit attributes (a full device simulation step 471 is performed, column 8, lines 46-54);

a simulation data store generator configured to:

create instances of a simulation data store, each simulation data store instance storing data elements comprising the profile data, associated measured signals, simulation types, and associated device attributes and circuit attributes (Output data that is generated by the calibration process 400 includes all of the matching profiles and all simulated profiles, column 9, lines 1-3; profiles and data which are entered into the database, column 12, lines 14-21);

wherein the simulation types are characterizations of the one or more device or circuit simulations performed (a plurality of suitable process steps is performed independently, column 6, lines 8-19; a full device simulation step 471 is performed, column 8, lines 46-54).

7-32. Regarding claim 38, Chen discloses a system for real-time determination of profile-based simulation information for an integrated circuit, the system comprising:

a query device configured to:

send a query comprising type of inquiry for profile-based simulation data and query given data (process parameters are acquired using the test equipment 212, column 4, lines 55-63), and

receive a response to the query (Acquired process parameter data are conveyed to the simulation computer system over a transmission path 216, column 4, lines 63-65);

a simulation data store server configured to:

process the query and formulate the response to the query (Acquired process parameter data are conveyed to the simulation computer system over a transmission path 216, column 4, lines 63-65); and

a simulation data store configured to:

store instances having data elements comprising profile data, signals, and process control parameters, and fabrication attributes (database 1020, column 12, lines 14-21);

wherein the simulation data store server, receiving a query from the query device, accesses selected instances of the simulation data store, the selection of the instances of the simulation data store determined by the type of inquiry and query given data, formulates the

response to the query, and transmits the response to the query device (automatic data extraction step 1022, column 12, lines 14-17).

7-33. Regarding claim 39, Chen further discloses wherein the query device is a metrology system and the query given data is a measured diffracted signal generated by the metrology system (test equipment 212 include laser reflectometry equipment and similar data acquisition tools that are known in the art of manufacturing, column 5, lines 6-11).

7-34. Regarding claim 40, Chen further discloses wherein the query given data is the measured diffracted signal and the response to the query comprises interconnect electrical device attributes from the selected instances of the simulation data store (automatic data extraction step 1022, column 12, lines 14-17).

7-35. Regarding claim 41, Chen further discloses wherein the query given data are process control parameters comprising focus and numerical aperture (test equipment 212 include spectroscopes and similar data acquisition tools that are known in the art of manufacturing, column 5, lines 6-11) and the response to the query are fabrication attributes comprising sidewall angle and top critical dimension from the selected instances of the simulation data store (automatic data extraction step 1022, column 12, lines 14-17).

7-36. Regarding claim 42, Chen further discloses wherein the query device, the simulation data store, and the simulation data store server are contained in one logical device (computer system 214, column 4, lines 55-58).

7-37. Regarding claim 43, Chen further discloses wherein the one logical device is coupled to one or more integrated circuit fabrication process devices (fabrication equipment 210, column 4, lines 55-58)

7-38. Regarding claim 44, Chen further discloses wherein the integrated circuit fabrication process device is a lithography unit (photolithography equipment, column 5, lines 2-6).

7-39. Regarding claim 45, Chen further discloses wherein the integrated circuit fabrication process device is a photoresist stripping unit (wafer cleaning equipment, column 5, lines 2-6).

7-40. Regarding claim 46, Chen discloses a computer-readable storage medium containing computer executable code to provide a response to an inquiry regarding profile-based simulation data of an integrated circuit by instructing the computer to operate as follows:

receiving a query from a query device, the query comprising a type of inquiry and query given data (process parameters are acquired using the test equipment 212, column 4, lines 55-63);

accessing a selected one or more instances of a simulation data store, the selection determined by the type of inquiry and query given data (automatic data extraction step 1022, column 12, lines 14-17); and

formulating a response to the query and transmitting the response to the query device (Acquired process parameter data are conveyed to the simulation computer system over a transmission path 216, column 4, lines 63-65);

wherein the simulation data store stores instances having data elements comprising structure profile data, fabrication attributes, signals, and process control parameters (database 1020, column 12, lines 14-21).

7-41. Regarding claim 47, Chen discloses a computer-readable storage medium containing computer executable code to create a profile-based simulation data store for an integrated circuit by instructing the computer to operate as follows:

performing a fabrication process simulation using process control parameters (A simulation start step 452 begins the simulation process 450 in response to initializing data from the actual in-line process 420, column 6, lines 36-54), the fabrication process simulation generating fabrication attributes and structure profile data (The generate simulated profile step 458 constructs a simulated profile, column 7, lines 36-41);

calculating a simulated signals for the structure profile data using a metrology simulator (A conversion operation is performed on the simulated profile in matching process conversion step 468, column 8, lines 4-25); and

creating an instance of a simulation data store, the instance of the simulation data store having data elements comprising the structure profile data, the associated fabrication attributes, the simulated signals, and the process control parameters (Output data that is generated by the calibration process 400 includes all of the matching profiles and all simulated profiles, column 9, lines 1-3; profiles and data which are entered into the database, column 12, lines 14-21).

7-42. Regarding claim 48, Chen discloses a computer-readable storage medium containing computer executable code to create a profile-based simulation data store for an integrated circuit by instructing the computer to operate as follows:

simulating one or more devices using a selected set of input parameters, the device simulations generating device attributes, the set of input parameters including profile data corresponding to the one or more simulated devices (a full device simulation step 471 is performed, column 8, lines 46-54);

generating calculated signals with a metrology simulator, the metrology simulator using profile data corresponding to the one or more simulated devices (A conversion operation is

performed on the simulated WET data in WET statistical profile conversion step 480, column 8, lines 54-67); and

creating simulation data store instances, the instances including calculated metrology signals, profile data, simulation types, process control parameters, and fabrication attributes (Output data that is generated by the calibration process 400 includes all of the matching profiles and all simulated profiles, column 9, lines 1-3; profiles and data which are entered into the database, column 12, lines 14-21);

wherein the simulation types are characterizations of the one or more simulations performed (a full device simulation step 471 is performed, column 8, lines 46-54).

7-43. Regarding claim 49, Chen discloses a computer-readable storage medium containing computer executable code to create a profile-based simulation data store for an integrated circuit by instructing the computer to operate as follows:

simulating one or more circuits using a selected set of input parameters, a circuit having one device, the circuit simulations generating circuit attributes, the set of input parameters including profile data corresponding to the one or more devices of the simulated one or more circuits (a full device simulation step 471 is performed, column 8, lines 46-54);

generating calculated signals with a metrology simulator, the metrology simulator using profile data corresponding to the one or more devices of the simulated one or more circuits (A conversion operation is performed on the simulated WET data in WET statistical profile conversion step 480, column 8, lines 54-67); and

creating simulation data store instances, the instances including calculated metrology signals, profile data, simulation types, process control parameters, and circuit attributes (Output

data that is generated by the calibration process 400 includes all of the matching profiles and all simulated profiles, column 9, lines 1-3; profiles and data which are entered into the database, column 12, lines 14-21);

wherein the simulation types are characterizations of the one or more simulations performed (a full device simulation step 471 is performed, column 8, lines 46-54).

7-44. Regarding claim 50, Chen discloses a method of providing a service for creating and using a profile-based simulation data store for an integrated circuit, the method comprising:

contracting by a client and a vendor, for the client to remunerate the vendor for the use of systems, processes, and procedures to create and use a profile-based simulation data store; and providing by the vendor to the client access to systems, processes, and procedures to create and use a profile-based simulation data store, the simulation data store storing instances having data elements comprising profile data, metrology signals, process control parameters, and fabrication attributes (database 1020, column 12, lines 14-21).

7-45. Regarding claim 51, Chen discloses a profile-based simulation data store for an integrated circuit, the data store comprising:

one or more instances of a simulation data store, each instance of the simulation data store including profile data, associated metrology signal and one or more simulation data segments (database 1020, column 12, lines 14-21);

wherein the metrology signal corresponds to an integrated circuit structure with a profile characterized by the profile data (A conversion operation is performed on the simulated WET data in WET statistical profile conversion step 480, column 8, lines 54-67);

wherein each data segment includes simulation type, associated process control parameters or associated simulation input parameters, and associated simulation attributes (Simulation results from the simulation steps 454, column 7, lines 31-36); and

wherein the associated simulation attributes comprises data determined by the simulation using the process control parameters or the associated simulation input parameters (Simulation results from the simulation steps 454, column 7, lines 31-36).

7-46. Regarding claim 52, Chen further discloses wherein the simulation attributes are fabrication process attributes, device attributes, or circuit attributes depending on the simulation type (Simulation results from the simulation steps 454, column 7, lines 31-36).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 10, 12, 14, 15, 17, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen, U.S. Patent 5,719,796 issued February 17, 1998, in view of Applicants' admission.

9-1. Regarding claim 10, Chen discloses a method of creating a profile-based simulation data store for an integrated circuit utilizing one or more simulations in claim 9. However, Chen fails to expressly disclose wherein the one or more circuits simulated include transmission lines, resistors, capacitors, inductors, amplifiers, switches, diodes, or transistors. Nevertheless, Chen

discloses performing a full device simulation in step 471 and generating a device profile that corresponds to the actual calculated WET data in step 473 (column 8, lines 46-54). In other words, to generate profile corresponding to the actual calculated WET data the device simulation or circuit simulation (e.g., a circuit may have one device) should be powerful enough to include simulation of any corresponding specific device or devices.

Applicants list examples of device simulators, interconnect simulators, circuit simulators, and combined simulators in the specification. Specifically, Applicants admit SPICE™ is an example of circuit simulator at paragraph [0041]. SPICE™ is well known in simulating various devices and circuits including transmission lines, resistors, capacitors, inductors, amplifiers, switches, diodes, transistors, as well as power devices and interconnects.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Chen to incorporate the assertions of Applicants to obtain the invention as specified in claim 10 because Chen suggest a full device simulation and SPICE™ is well known in circuit simulation including device simulation.

9-2. Regarding claim 12, Chen discloses a method of creating a profile-based simulation data store for an integrated circuit utilizing one or more simulations in claim 11. Chen further discloses wherein the one or more fabrication processes simulated include a lithography simulation and an etch simulation (photolithography and wet etching equipment, column 5, lines 2-6). However, Chen fails to expressly disclose the one or more device simulations include an interconnect simulation. Nevertheless, Chen discloses performing a full device simulation in step 471 and generating a device profile that corresponds to the actual calculated WET data in step 473 (column 8, lines 46-54). In other words, to generate profile corresponding to the actual

calculated WET data the device simulation or circuit simulation (e.g., a circuit may have one device) should be powerful enough to include simulation of any corresponding specific device or devices.

Applicants list examples of device simulators, interconnect simulators, circuit simulators, and combined simulators in the specification. Specifically, Applicants admit SPICE™ is an example of circuit simulator at paragraph [0041]. SPICE™ is well known in simulating various devices and circuits including transmission lines, resistors, capacitors, inductors, amplifiers, switches, diodes, transistors, as well as power devices and interconnects.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Chen to incorporate the assertions of Applicants to obtain the invention as specified in claim 12 because Chen suggest a full device simulation and SPICE™ is well known in circuit simulation including device simulation.

9-3. Regarding claims 14 and 15, Chen discloses a method of creating a profile-based simulation data store for an integrated circuit in claim 13. However, Chen fails to expressly disclose the one or more device simulations include (1) a power device simulation and an interconnect simulation, or (2) a transmission line simulation and an amplifier simulation. Nevertheless, Chen discloses performing a full device simulation in step 471 and generating a device profile that corresponds to the actual calculated WET data in step 473 (column 8, lines 46-54). In other words, to generate profile corresponding to the actual calculated WET data the device simulation or circuit simulation (e.g., a circuit may have one device) should be powerful enough to include simulation of any corresponding specific device or devices.

Applicants list examples of device simulators, interconnect simulators, circuit simulators, and combined simulators in the specification. Specifically, Applicants admit SPICE™ is an example of circuit simulator at paragraph [0041]. SPICE™ is well known in simulating various devices and circuits including transmission lines, resistors, capacitors, inductors, amplifiers, switches, diodes, transistors, as well as power devices and interconnects.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Chen to incorporate the assertions of Applicants to obtain the invention as specified in claims 14 and 15 because Chen suggest a full device simulation and SPICE™ is well known in circuit simulation including device simulation.

9-4. Regarding claim 17, Chen discloses a method of creating a profile-based simulation data store for an integrated circuit utilizing one or more simulations in claim 16. Chen further discloses wherein the one or more fabrication process simulations include a lithography simulation (photolithography equipment, column 5, lines 2-6). However, Chen fails to expressly disclose the one or more device simulation includes an interconnect simulation, and the one or more circuit simulation include a transmission line simulation. Nevertheless, Chen discloses performing a full device simulation in step 471 and generating a device profile that corresponds to the actual calculated WET data in step 473 (column 8, lines 46-54). In other words, to generate profile corresponding to the actual calculated WET data the device simulation or circuit simulation (e.g., a circuit may have one device) should be powerful enough to include simulation of any corresponding specific device or devices.

Applicants list examples of device simulators, interconnect simulators, circuit simulators, and combined simulators in the specification. Specifically, Applicants admit SPICE™ is an

example of circuit simulator at paragraph [0041]. SPICE™ is well known in simulating various devices and circuits including transmission lines, resistors, capacitors, inductors, amplifiers, switches, diodes, transistors, as well as power devices and interconnects.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Chen to incorporate the assertions of Applicants to obtain the invention as specified in claim 17 because Chen suggest a full device simulation and SPICE™ is well known in circuit simulation including device simulation.

9-5. Regarding claim 20, Chen discloses a method of creating a profile-based simulation data store for an integrated circuit in claim 18. However, Chen fails to expressly disclose wherein the one or more device simulations are interconnect simulations. Nevertheless, Chen discloses performing a full device simulation in step 471 and generating a device profile that corresponds to the actual calculated WET data in step 473 (column 8, lines 46-54). In other words, to generate profile corresponding to the actual calculated WET data the device simulation or circuit simulation (e.g., a circuit may have one device) should be powerful enough to include simulation of any corresponding specific device or devices.

Applicants list examples of device simulators, interconnect simulators, circuit simulators, and combined simulators in the specification. Specifically, Applicants admit SPICE™ is an example of circuit simulator at paragraph [0041]. SPICE™ is well known in simulating various devices and circuits including transmission lines, resistors, capacitors, inductors, amplifiers, switches, diodes, transistors, as well as power devices and interconnects.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Chen to incorporate the assertions of Applicants to obtain

the invention as specified in claim 20 because Chen suggest a full device simulation and SPICE™ is well known in circuit simulation including device simulation.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to Applicant's disclosure.

Reference to Tegethoff, U.S. Patent 5,539,652 issued July 23, 1996, is cited as disclosing a method for manufacturing test simulation in electronic circuit design.

Reference to Niu et al., U.S. Patent 6,433,878 B1 issued August 13, 2002, and filed January 29, 2001, is cited as disclosing a method for the determination of mask rules using scatterometry.

Reference to Bao et al., U.S. Patent 6,609,086 B1 issued August 19, 2003, and filed February 12, 2002, is cited as disclosing profile refinement for integrated circuit metrology.

Reference to Jakadar et al., U.S. Patent 6,694,275 B1 issued February 17, 2004, and filed November 28, 2000, is cited as disclosing a profiler model.

Reference to Chang et al., U.S. Patent 6,757,645 B2 issued June 29, 2004, and filed August 7, 1998, is cited as disclosing a visual inspection and verification system.

Reference to Jakadar et al., U.S. Patent 6,768,983 B1 issued July 27, 2004, and filed November 28, 2000, is cited as disclosing a method for real-time library generation of grating profiles.

Reference to Wang et al., U.S. Patent 6,968,303 B1 issued November 22, 2005, and filed April 13, 2000, is cited as disclosing a method for extracting and combining tool trace data and WET data for semiconductor processing.

11. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Herng-der Day whose telephone number is (571) 272-3777. The Examiner can normally be reached on 9:00 - 17:30.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: (571) 272-2100.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Kamini S. Shah can be reached on (571) 272-2279. The fax phone numbers for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Herng-der Day
February 6, 2006

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